16966

Normally-off 4H-SiC trenched gate MOSFETs with high mobility

J. Wu [a], J. Hu [a], J. H. Zhao [a], X. Wang [b], X. Li [b], L. Fursin [b], T. Burke [c]

[a] SiCLAB, Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 08901, USA.
[b] United Silicon Carbide, Inc., 100 Jersey Ave, Bldg. A., New Brunswick, NJ 08901, USA.
[c] U.S. Army TACOM, Warren, MI 48397, USA.

Abstract

A normally-off 4H-SiC trenched gate MOSFET structure with epitaxial buried channel, coupled with improved fabrication processes has resulted in substantially improved channel mobility. Fabricated devices subject to high-temperature ohmic contact rapid thermal annealing at 850 °C for 5 min exhibit a peak field-effect mobility (μ_{FE}) of 95 cm^2/Vs at room temperature (25 °C) and 255 cm^2/Vs at 200 °C, which are among the highest reported to date. The dependence of channel mobility and threshold voltage on buried channel depth is investigated to explore the optimum range of channel depth.

Keywords: 4H-SiC; Tenched gate MOSFETs; Mobility

PACS CODES: 85.30.Tv

1. Introduction:

Silicon carbide (SiC) power devices are expected to drastically outperform Si counterparts due to the superior physical properties of SiC, such as wide bandgap, high breakdown field and high thermal conductivity. In particular, the 4H-SiC MOSFET is a key component in future power switching applications to meet

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
28 FEB 2007	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Normally-off 4H-SiC trenched gate MOSFETs with high mobility	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
J. Hu; J. Wu; J.H. Zhao; X. Wang; X. Li; L. Fursin; T. Burke	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
US Army RDECOM-TARDEC 6501 E 11 Mile Rd Warren, MI 48397-5000 SiCLAB, Department of Electrical and ComputerEngineering, Rutgers University, 94 Brett Road, Piscataway,NJ 08901, USA United Silicon Carbide, Inc., 100 Jersey Ave. Bldg. A., New Brunswick, NJ 08901	**#16966**
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	TACOM/TARDEC
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)
	#16966

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
Sent for publication to IEEE Electron Device Letters

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**SAR**	**15**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

increasing demands of handling higher power densities at temperatures possibly up to 200°C. At present, however, the development of 4H-SiC MOSFETs have been hampered by notorious channel mobility and gate oxide reliability problems. The major reason for low channel mobility is believed to be the presence of the exponentially increased interface states towards the conduction band edge, resulting in substantial electron trapping and Coulomb scattering at the SiO_2/SiC interface [1]. Besides, interface surface roughness may also play a major role in affecting channel mobility through scattering of the electrons by collision. In typical SiC-MOSFETs, the source region is formed by a heavy implantation followed by activation annealing higher than 1500°C, which make the flat surface of SiC rough. The fact that gate oxide is usually formed on the source region with substantial surface roughness also gives rise in the concerns of gate oxide reliability. Hence we believe the substantial surface roughness is the ultimate bottleneck in limiting the gate oxide reliability as well as the channel mobility. Recently, various approaches have been employed to improve the quality of the MOS interface [2-7]. Peak inversion channel mobilities of 50~70 cm^2/Vs [3, 4] have been obtained by the nitridation of SiO_2/SiC interface through nitric oxide (NO) growth or NO annealing. Even higher high inversion channel mobility up to 150 cm^2/Vs has been achieved by the use of contaminated alumina environment for gate oxidation [5]. However, two factors might make this special process not suitable for MOSFET fabrication: Rapid thermal annealing for ohmic contacts has to be excluded for attaining the above results, or the channel mobility can be decreased by a factor of about two [6]; Substantial mobile ions have been introduced into gate oxide under the contaminated alumina environment. In addition, some researchers utilized a buried channel structure formed by ion implantation to improve the channel mobility in 4H-SiC MOSFETs up to 140 cm^2/Vs

[7]. Similar to [5], however, this high mobility was only obtained without high-temperature contact annealing.

In this paper a 4H-SiC lateral trenched gate MOSFET with very high channel mobility is reported. Unlike all published works [3-8], the structure of lateral trenched gate MOSFET contains the novel features aiming at improving channel mobility and gate oxide reliability: no N^+ source implantation and hence no high-temperature ($\geq$1500 ^{o}C) surface-degrading activation annealing are introduced in fabrication; no epitaxial regrowth is required; no MOS channel implantation. In addition, the study of the lateral trenched gate MOSFET is part of an on-going effort in developing vertical power MOSFETs, where all the advantages described above can be transferred into reliable power MOSFETs with low on-resistance. This paper will report the result of the successful demonstration of very high channel mobility for the lateral MOSFET. The dependence of channel mobility and threshold voltage on buried channel depth is also studied to explore the optimum channel depth.

2. Device fabrication

The cross-sectional view of a fabricated 4H-SiC lateral trench-gate MOSFET is presented in Fig.1. As shown, if the dotted p-type region is converted into n-type by a low dose ion implantation, the lateral structure can be easily transformed into a vertical power MOSFET. The channel length to width ratio of the device is 15 μm / 350 μm. The starting 4H-SiC 8^{o} off-axis Si face commercial wafer had an initial 0.22 μm thick N-type epilayer with a doping concentration of $2x10^{16}$ cm^{-3} as the buried channel, a 0.90 μm $4x10^{17}$ cm^{-3} doped P-type epilayer underneath the channel layer, and a highly doped N^+ cap epilayer (0.15 μm, N_d=$2x10^{19}$ cm^{-3}) for implant-free source ohmic contact. The wafer was first etched by inductively-coupled plasma (ICP) in the

CF_4/O_2 mixture into p-type epilayer for mesa isolation. Thereafter, three trenched-gate regions with different depths of 0.15, 0.12 and 0.09 μm were then formed by shallow ICP etching, in order to investigate the dependence of channel mobility and threshold voltage on buried channel depth. A sacrificial oxide layer was then thermally grown in wet ambient at 1100 °C for 0.5 hr and then stripped off by diluted HF acid. The gate oxide was grown first in nitric oxide (NO) at 1175 °C, followed by NO annealing at 950 °C and further oxidation in dry O_2 at 1175 °C plus a final oxidation in NO at 1175 °C, resulting in a total gate oxide thickness of 100nm. After opening windows into the oxide, 300nm thick Ni was sputtered to form source and drain contacts. Rapid thermal annealing for ohmic contacts was performed at 850 °C for 5 min in nitrogen forming gas (5% H_2 in N_2), which is a critical step for future vertical power MOSFET fabrication. Gate contacts were formed by a 300 nm thick layer of Mo.

Based on device structure shown in Fig.1 and above fabrication process, it is seen that source region is formed by epitaxial N^+ layer instead of heavily implanted N^+ region, which hence excludes high temperature activation annealing (≥1500 °C). The preserved SiC flat surface would alleviate the concerns on channel mobility and gate oxide reliability. Although low dose implantation will be introduced in the fabrication of vertical power MOSFETs, only low temperature activation annealing (<1500 °C) is used. In addition, buried MOS channel is formed by N epitaxial layer so that neither epitaxial regrowth nor channel implantation is introduced. The expitaxial buried channel layer would contribute to the improvement of the channel mobility by keeping electrons conduction flow away from the SiO2/SiC surface to reduce interfacial trapping effects on carrier mobility.

3. Results and discussion

Characterizations were conducted with a HP4145B semiconductor parameter analyzer. All the devices were tested at chip level using a standard probe station with source contacts grounds. The gate leakage between the gate and drain contacts was first measured and confirmed to be in pA range. The results presented in the paper were collected from MOSFETs with channel current flow perpendicular to the wafer's major flat, since such devices were always found to exhibit relatively higher output currents.

The output I_{DS}-V_{DS} characteristics of a device at room temperature (25 °C) and 200 °C are shown in Fig. 2a and Fig. 2b, respectively. The gate voltage was stepped in 10 V step up to 40 V, corresponding to a high electric field of 4 MV/cm across the gate oxide. It is very clear that the drain currents at 200 °C are drastically higher compared to those at room temperature, indicating substantially increased channel mobility at 200 °C. Fig. 3a and Fig. 3b show the transfer I_{DS}-V_{GS} characteristics of a device measured with V_{DS} = 50 mV at room temperature and 200 °C. The corresponding field-effect mobility μ_{FE} was calculated from equation (1) and also plotted in Fig. 3a and Fig.3b.

$$\mu_{FE} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{1}{C_{OX} V_{DS}} \left(\frac{L}{W} \right) \tag{1}$$

In the above equation, C_{OX} is the oxide capacitance, and L and W are the channel length and width respectively. Fig. 3a shows μ_{FE} at room temperature reaches a peak value as high as 95 cm^2/Vs around the electric field of 1 MV/cm, representing a significant improvement in the channel mobility at room temperature as compared to that in [3, 4] subjected to similar high-temperature ohmic contact rapid thermal annealing. It is worth point out that this result is more meaningful for fabrication of MOSFETs compared to those higher mobilities of 140~150 cm^2/Vs in [5-7], because those results could be only obtained without ohmic contact annealing. It can be also

inferred that the buried-channel, epitaxially grown with superior quality in comparison to implanted channel, effectively reduces the influence of interface traps and surface roughness by keeping the electron flow further away from the interface. The calculated μ_{FE} at 200 °C as a function of V_{GS} shown in Fig. 3b exhibits a substantially higher peak value of 255 cm^2/Vs around a low electrical field of 1 MV/cm as compared to that at room temperature. The increase of the channel mobility with increasing temperature, which was also reported in [3], can be attributed to thermal detrapping of electrons. The reduced Coulomb scattering due to the detrapping leads to higher channel mobility which, on top of increased channel electron concentration, result in the drastic increase in the MOSFET drain current as shown in Fig. 2b. On the other hand, in power MOSFETs the increased channel mobility at elevated temperature can be useful to compensate the increased on-resistant of low-dose drift layer at elevated temperature due to phonon scattering. Revisiting both Fig. 3a and Fig. 3b, it is seen that the μ_{FE} decreases from the peak value as gate oxide electric field is increased. It is an expected phenomenon because at high gate oxide electric field channel electrons are drawn very closer to the SiO_2/SiC interface, where the interface traps as well as surface roughness give rise to much stronger scattering of the electron flow. Threshold voltage (V_{th}) is extracted from the intercept on the V_{GS} axis of Fig. 3a and Fig. 3b by a linear fit. V_{th} at room temperature is found to be 5.3 V, showing a clear normally-off operation. V_{th} at 200 °C is extracted to be 5.1 V from the I_{DS}-V_{GS} curve in Fig. 3b, still showing a stable normally-off operation.

The depth of expitaxial buried channel (D_{ch}) is an important parameter for trenched gate MOSFETs. In addition to the devices with 0.15 μm thick buried channel, the devices with 0.12 and 0.09 μm thick buried channel were fabricated on the same chip

and tested in the same procedure as above. Fig. 4 shows the dependence of the peak μ_{FE} on buried channel depth at room temperature and 200 °C. For the channel depth of 0.09, 0.12, and 0.15 μm, the peak μ_{FE} values are 59, 81, and 95 cm^2/Vs at room temperature, respectively. The significant improvement of channel mobility with increase of channel depth is also discovered at the device temperature of 200 °C, i.e., 160, 190, and 255 cm^2/Vs for the channel depth of 0.09, 0.12, and 0.15 μm respectively. This tendency can be interpreted that as channel depth increases more electrons can flow in the deep position away from the SiO_2/SiC interface with less scattering of interface traps and surface roughness. At each channel depth the devices always show much higher channel mobility at 200 °C than that at room temperature because of thermal detrapping of electrons. It can be then inferred that surface roughness scattering dominates at elevated temperature of 200 °C. The dependence of the threshold voltage on buried channel depth at room temperature and 200 °C are compared in Fig. 5. It is seen that threshold voltage decreases due to the extension of channel depth. For the channel depth of 0.09, 0.12, and 0.15 μm, the threshold voltages are 25.3, 14.6, and 5.3 V respectively at room temperature, 14, 10.4, and 5.3 cm^2/Vs respectively at 200 °C, all indicating normally-off operation. The decrease of V_{th} with extended D_{ch} can be attributed to less pinch-off of buried channel in thicker buried channel. Fig.5 also shows for each channel depth, V_{th} is always higher at elevated temperature of 200 °C as compared to that at room temperature, which is consistent with the detrapping of negative electrons at the channel interface. However, the devices with different D_{ch} show substantial discrepancy on the variation of V_{th} at room temperature and 200 °C. The device with D_{ch} of 0.15 μm only shows the shift of V_{th} as small as 0.2 V, whereas the device with D_{ch} of 0.09 μm exhibits a big shift of 11.3 V. It can be inferred that in thicker buried channel thermal detrapping of

electrons would give rise to weaker influence on V_{th}. Based on the analysis on Fig. 4 and Fig. 5, it can be concluded that D_{ch} of 0.15 μm is most optimized channel depth among three regions, which gives the device the highest mobility at both room temperature and 200 °C and limit the shift of V_{th} to the smallest.

The high channel mobility result reported in this paper is being used in the on-going fabrication of vertical power MOSFETs having a structure similar to Fig.1 except the dotted, shadowed p region is converted to n region by low dose nitrogen implant with lower temperature (<1500 °C) activation annealing which preserves a near virgin epilayer surface to ensure high channel mobility and high gate oxide reliability.

4. Conclusion

A high channel mobility lateral 4H-SiC trenched gate MOSFET has been demonstrated. The fabricated devices with a channel depth of 0.15 μm, even after undergoing the rapid thermal annealing at 850 °C for ohmic contacts, still exhibit a high channel mobility of 95 cm^2/Vs at room temperature and 255 cm^2/Vs at 200 °C with a clear normally-off operation. To the best of our knowledge, this value is among the highest reported to date for a normally-off 4H-SiC MOSFET that has undergone high temperature rapid thermal annealing. This result makes it possible to develop vertical power MOSFET with the novel features of (i) no high-dose ion implantation, (ii) no ≥1500°C high-temperature surface-degrading activation annealing, (iii) no N^+ source implantation and hence no gate oxide on top of heavily implanted source region, (iv) no epitaxial regrowth, and (v) no MOS channel implantation, all aimed at improving channel mobility and gate oxide reliability. In addition, the dependence of channel mobility and threshold voltage on buried channel depth has been investigated

and compared to conclude that the channel depth of 0.15 μm is close to the optimized range for highest channel mobility and smallest threshold voltage shift.

References

[1] Cooper JA, Melloch MR, Singh R, Agarwal A, Palmour JW. Status and prospects for SiC power MOSFETs. IEEE Trans Electron Dev 2002;49:658-64.

[2] Lipkin LA, Das MK, Palmour JW. N_2O processing improves the 4H-SiC: SiO_2 interface. Mat Sci Forum 2002;389-393:985.

[3] Lu CY, Cooper JA, Tsuji T, Chung G, Williams JR, McDonald K, et al. Effect of process variations and ambient temperature on electron mobility at the SiO_2/4H-SiC interface. IEEE Trans Electron Devices 2003;50;1582-88.

[4] Das MK. Recent Advances in (0001) 4H-SiC MOS Device Technology. Mat Sci Forum 2004;457-460:1275-80.

[5] Ólafsson HÖ, Gudjónsson G, Allerstam F, Sveinbjörnsson EÖ, Rödle T, Jos R. Stable operation of high mobility 4H-SiC MOSFETs at elevated temperatures. Electron Lett 2005;41:825-6.

[6] Gudjónsson G, Ólafsson HÖ, Allerstam F, Nilsson P-Å, Sveinbjörnsson EÖ, Zirath H, et al. High field-effect mobility in n-channel Si face 4H-SiC MOSFETs with gate oxide grown on aluminum ion-implanted material. IEEE Electron Dev Lett 2005;26:96-8.

[7] Harada S, Suzuki S, Senzaki J, Kosugi R, Adachi K, Fukuda K, et al. High channel mobility in normally-off 4H-SiC buried channel MOSFETs, IEEE Electron Dev Lett 2001;22;272-4.

[8] Harada S, Okamoto M, Yatsuo T, Adachi K, Suzuki K, Suzuki S, et al. Fabrication of 4H-SiC Double-Epitaxial MOSFETs. Mat Sci Forum 2004;457-460:1421-4.

Figure captions:

Fig. 1. Cross-sectional view of lateral 4H-SiC trenched gate MOSFET which can be readily converted into vertical power MOSFET by converting the dotted p-region into n-region through a lower dose implant with a lower temperature activation annealing .

Fig. 2. Output characteristics of the lateral 4H-SiC trenched gate MOSFET (Forward I_{ds} versus V_{ds} at different V_{gs}) (a) at room temperature; (b) at 200 °C.

Fig. 3. Transfer characteristics (I_{ds} versus V_{gs}) of the lateral 4H-SiC trenched gate MOSFET at V_{ds} of 50 mV, and field-effect mobility as a function of gate voltage (a) at room temperature; (b) at 200 °C..

Fig. 4. Peak field effect mobility V_{th} as a function of buried channel depth D_{ch} at room temperature and 200 °C.

Fig. 5. Threshold voltage V_{th} as a function of buried channel depth D_{ch} at room temperature and 200 °C.

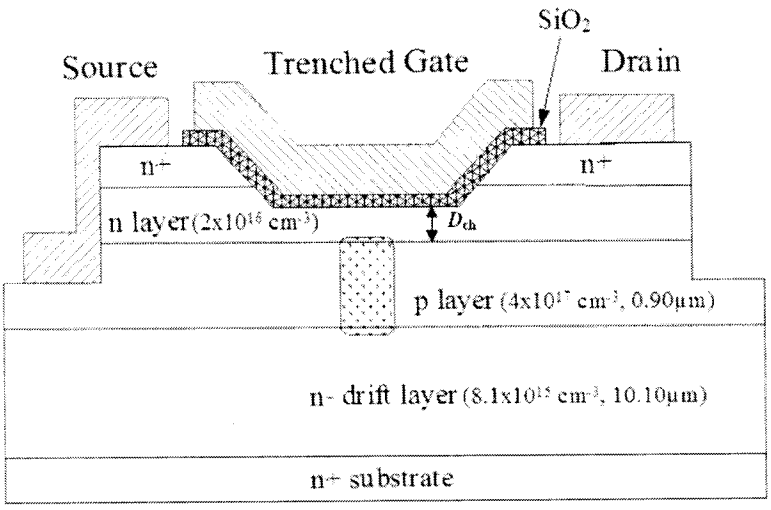

Fig. 1. Cross-sectional view of lateral 4H-SiC trenched gate MOSFET which can be readily converted into vertical power MOSFET by converting the dotted p-region into n-region through a lower dose implant with a lower temperature activation annealing.

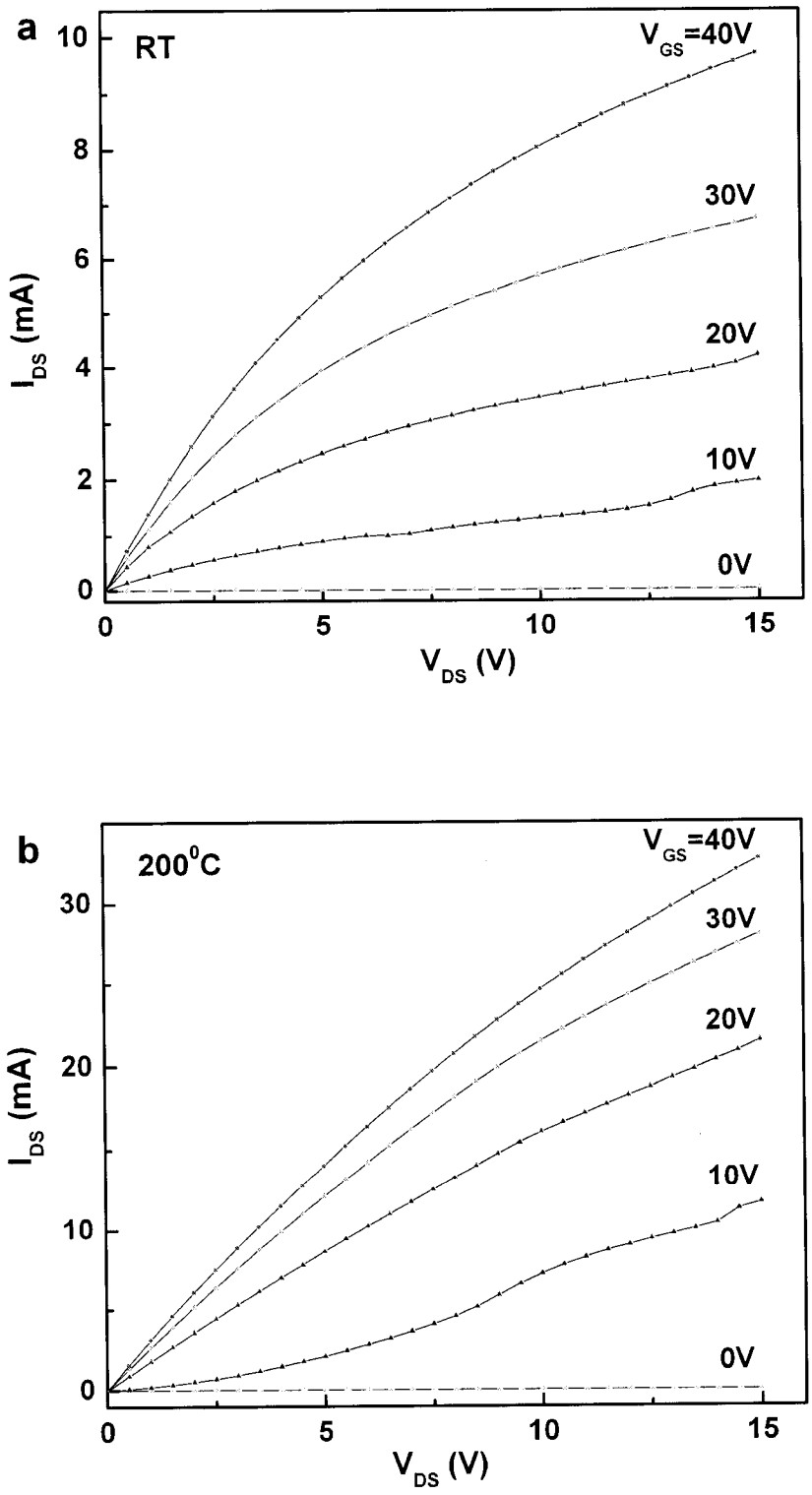

Fig. 2. Output characteristics of the lateral 4H-SiC trenched gate MOSFET (Forward I_{DS} versus V_{DS} at different V_{GS}) (a) at room temperature; (b) at 200 °C

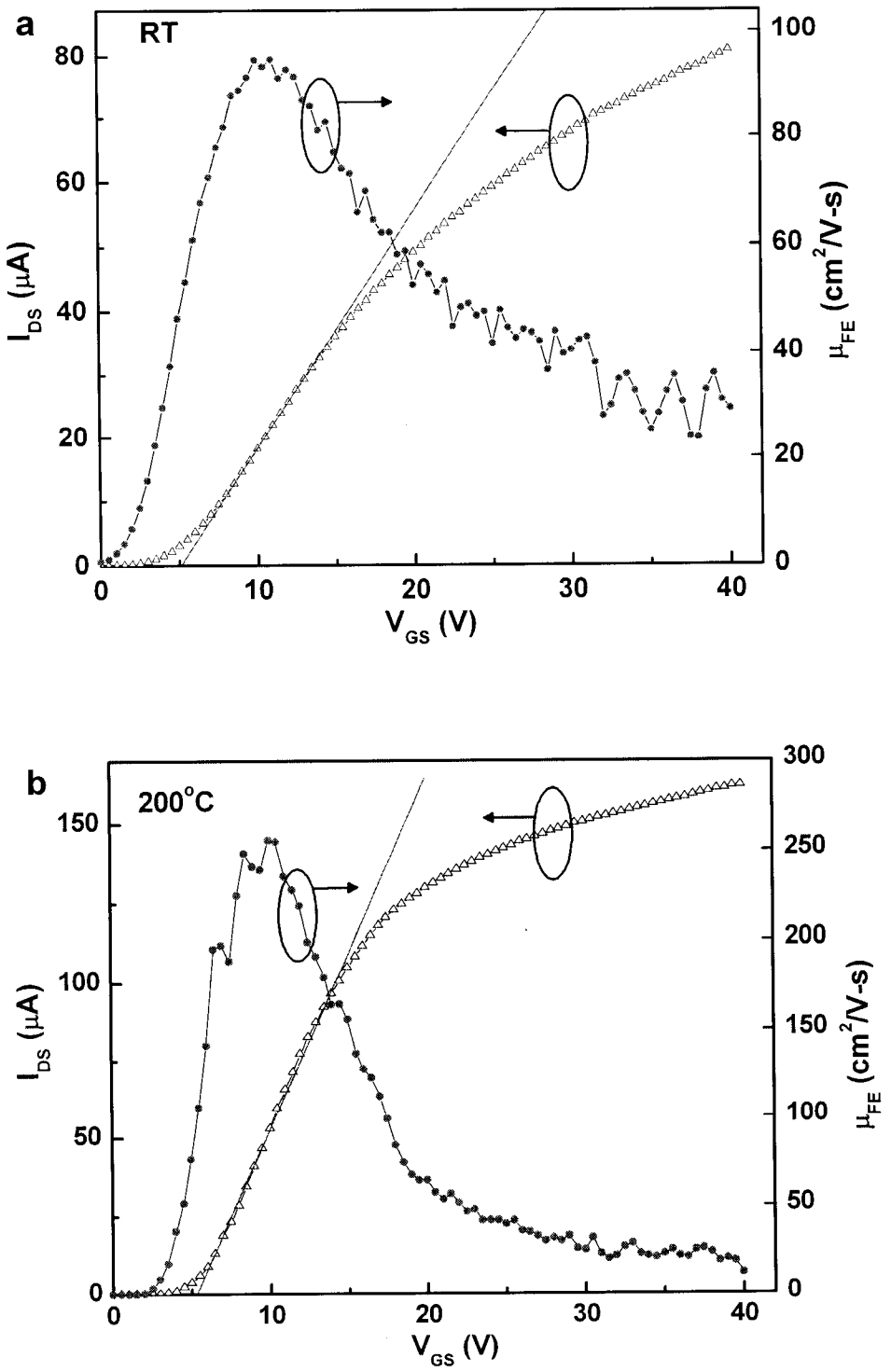

Fig. 3. Transfer characteristics (I_{DS} versus V_{GS}) of the lateral 4H-SiC trenched gate MOSFET at V_{DS} of 50 mV, and field-effect mobility as a function of gate voltage (a) at room temperature; (b) at 200 °C.

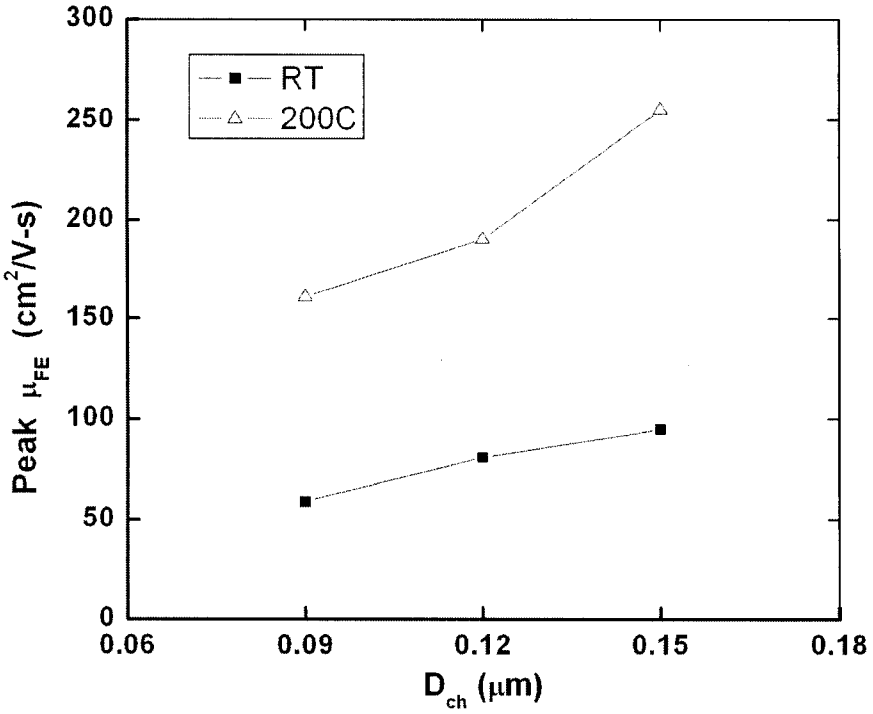

Fig. 4. Peak field effect mobility V_{th} as a function of buried channel depth D_{ch} at room temperature and 200 °C.

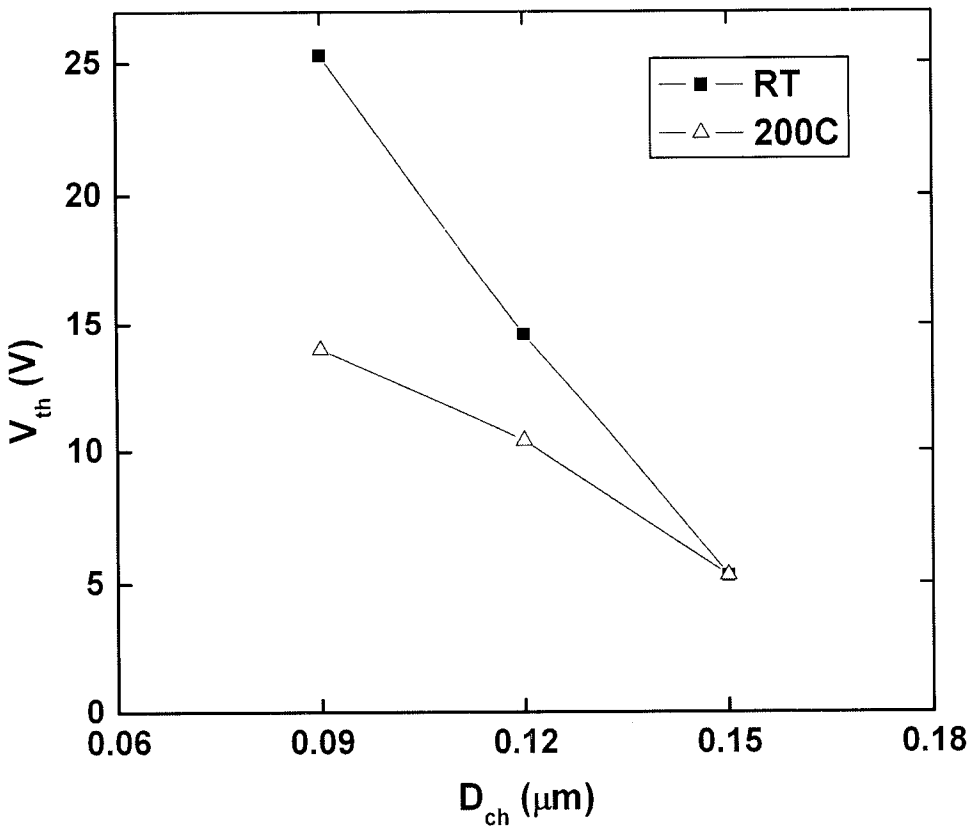

Fig. 5. Threshold voltage *V*th as a function of buried channel depth *D*ch at room temperature and 200 °C.